1. A method for modeling a memory with delay back annotation in accordance with the VITAL application specific integrated circuit modeling specification, the method comprising the step of:

modeling a path delay of said memory by overloading VITAL path delay procedures to provide path delay calculations for timing of address, control, and data bus signals to the memory.

2. The method of claim 1 further comprising the steps of:

modeling said memory with a timing generic and a port;

modeling a wire delay of said memory;

modeling a timing check for said memory;

modeling functioning of said memory.

3. The method of claim 1 wherein modeling of said path delay comprises the step of overloading VITAL timing check procedures for determining timing constraint violations of the timing of the address, control, and data bus signals of said memory.

4. The method of claim 1 wherein modeling of said path delay comprises the step of overloading VITAL wire delay procedures for determining interconnection delay of the address, control, and data bus signals of said memory.

5. The method of claim 1 wherein the memory is selected from a grouping of memories consisting of SRAM and Flash NVRAM.

6. An apparatus for modeling a memory with delay back annotation in accordance with the VITAL application specific integrated circuit modeling specification, the apparatus comprising:

means for modeling a path delay of said memory by overloading VITAL path delay procedures to provide path delay calculations for timing of address, control, and data bus signals to the memory.

7. The apparatus of claim 6 further comprising:

means for modeling said memory with a timing generic and a port;

means for modeling a wire delay of said memory;

means for modeling a timing check for said memory;

means for modeling functioning of said memory.

8. The apparatus of claim 6 wherein the means for modeling of said path delay comprises means for overloading VITAL timing check procedures for determining timing constraint violations of the timing of the address, control, and data bus signals of said memory.

9. The apparatus of claim 6 wherein the means for modeling of said path delay comprises means for overloading VITAL wire delay procedures for determining

interconnection delay of the address, control, and data bus signals of said memory.

10. The apparatus of claim 6 wherein the memory is selected from a grouping of memories consisting of SRAM and Flash NVRAM.

11. An electronic design automation system for modeling a memory with delay back annotation in accordance with the VITAL application specific integrated circuit modeling specification, the electronic design automation system:

a model library storage device which retains a model of a path delay of said memory, said model of said path delay including an overloading VITAL path delay procedures to provide path delay calculations for timing of address, control, and data bus signals to the memory, said model library storage device connected to an electronic design automation program execution unit that simulates the path delay of said memory.

12. The electronic design automation system of claim 11 further comprising:

a hardware description language storage device connected to the electronic design automation program execution unit, said hardware description language storage device retaining:

models of said memory with a timing generic and a port;

models of a wire delay of said memory;

models of a timing check for said memory;

models of functioning of said memory; and

13. The electronic design automation system of claim 11 wherein the models of said path delay comprise an overloading of VITAL timing check procedures for determining timing constraint violations of the timing of the address, control, and data bus signals of said memory.

14. The electronic design automation system of claim 11 wherein the models of said path delay comprises an overloading of VITAL wire delay procedures for determining interconnection delay of the address, control, and data bus signals of said memory.

15. The electronic design automation system of claim 11 wherein the memory is selected from a grouping of memories consisting of SRAM and Flash NVRAM.

16. A medium for retaining a computer program which, when executed on a computing system, executes an electronic design automation process that describes, evaluates, and simulates a model of a memory with delay back annotation in accordance with the VITAL application specific integrated circuit modeling specification, said electronic design automation process comprising the step of:

modeling a path delay of said memory by overloading VITAL path delay procedures to provide path delay calculations for timing of address, control, and data bus signals to the memory.

17. The medium of claim 16 wherein said electronic design automation process further comprises the steps of:

modeling said memory with a timing generic and a port;

modeling a wire delay of said memory;

modeling a timing check for said memory;

modeling functioning of said memory.

18. The medium of claim 16 wherein modeling of said path delay comprises the step of overloading VITAL timing check procedures for determining timing constraint violations of the timing of the address, control, and data bus signals of said memory.

19. The medium of claim 16 wherein modeling of said path delay comprises the step of overloading VITAL wire delay procedures for determining interconnection delay of the address, control, and data bus signals of said memory.

20. The medium of claim 16 wherein the memory is selected from a grouping of memories consisting of SRAM and Flash NVRAM.